ABSTRACT OF THE DISCLOSURE

A find-instructions-and-allocate-ports (FIAP) circuit and method are provided for quickly and efficiently locating one or more instructions that are ready for execution during a launch cycle in an out of order processor and allocating one or more ports associated with one or more execution resources to such ready instructions during the launch cycle. In architecture, the processor includes an instruction reordering mechanism, for example, a queue, having a plurality of slots for temporarily storing a plurality of respective instructions. Instructions can be executed in an out of order sequence from the queue. Each slot is provided with the FIAP circuit for causing and preventing launching, when appropriate, of their respective instruction. A plurality of signals is propagated successively through the FIAP circuits of the queue that causes the queue to launch a predefined plurality of the instructions, which corresponds to a predefined plurality of ports associated with the one or more execution resources. As propagation of the set of signals occurs through each slot, the set of signals indicates to the slot when and which of the one or more ports are available for each said instruction and when none of the ports are available.